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EVALUATION OF THE EFFECT OF HIGH-K MATERIALS ON THE PERFORMANCE OF CARBON NANOTUBE FIELD-EFFECT TRANSISTORS (CNTFETs)

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ABSTRACT
The increasing need of miniaturization, functionality, performance, and low cost have been the attractive force towards the use of high-k dielectrics as they provide crucial functions in integrated circuit as gate dielectrics, with their performance demands becoming more and more stringent as feature sizes decrease and speeds rise. This study investigates the impact of high-k dielectric materials on the electrical performance of Carbon Nanotube Field-Effect Transistors (CNTFETs) using the Field Effect Transistor Toy (FETToy) simulator. Six gate dielectrics; SiO_2 , Al_2O_3 , Y_2O_3 , Ta_2O_5 , HfO_2 , and La_2O_3 were evaluated under identical structural conditions, including a 1nm nanotube diameter, 1.5nm gate oxide thickness, and 1V drain bias at 300K. The simulation focused on key performance parameters such as drain current (Id), quantum capacitance (C_q), carrier velocity, mobile charge, quantum-to-insulator capacitance ratio (C_q/C_{ins}), and transconductance-to-current ratio (gm/Id). Results show that the use of high-k dielectric material significantly enhances the drain current, carrier velocity, and charge density, indicating improved gate coupling and electrostatic control. Among all the evaluated materials, La_2O_3 exhibited superior performance with the highest ON-current (77.5 μA), greatest carrier velocity (5.92×10^6 cm/s), and strongest gate control, while SiO_2 showed the weakest behavior across most metrics with lowest ON-current (30μA), lowest carrier velocity(4.2×10^6cm/s) and lowest value of 4.46×10^6 mobile charge/(q/cm). The analysis further reveals the need for balanced dielectric selection to optimize switching speed and energy efficiency. These findings confirmed that La_2O_3 is a promising dielectric for high-performance CNTFET applications in the next-generation nanoelectronic circuits.

Keywords: Carbon Nanotube Field Effect Transistors (CNTFETs), H-k dielectrics, On-current and Quantum Capacitance

1.0 INTRODUCTION
The continuous scaling of transistors remains a key driver behind the rapid advancement of Complementary Metal–Oxide–Semiconductor (CMOS) technology. However, the miniaturization of silicon-based devices has become increasingly challenging [1]. As the gate layers of silicon dioxide (SiO_2) become extremely thin, electron tunneling results in excessive power dissipation and leakage current, which has prompted the search for alternative materials [2]. To achieve higher levels of scaling than those attainable with traditional silicon Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs), new materials and device architectures have been explored. The introduction of high-k dielectric materials has represented a significant breakthrough, as they effectively reduce leakage current and allow improved charge injection, thereby sustaining performance and miniaturization in advanced CMOS technologies [3], [4]. Industrial projections indicate that this transition will continue to play a central role in future semiconductor technologies [5].

For accurate modeling and design of Carbon Nanotube Field-Effect Transistors (CNTFETs), reliable simulation tools are essential, since device performance strongly depends on the dielectric properties of the gate as well as the source and drain regions [6]. The incorporation of high-k dielectric materials into CNTFETs is critical to achieving lower operating voltages, higher ON-state currents, and reduced leakage, while maintaining subthreshold swing values close to the theoretical limit [7]. Nonetheless, CNTFETs are often limited by relatively low drain currents, and the use of high-k dielectrics as gate insulators offers a promising solution. These materials not only mitigate gate leakage but also enhance current drive, leading to improvement of the overall device performance [8].

Several studies have investigated different high-k dielectric materials and their impact on CNTFET behavior. For instance, the integration of zirconium oxide (ZrO_2) with carbon nanotubes through atomic-layer deposition has been reported to yield high-capacitance gate insulators [9]. The performance of CNTFETs using SiO_2, ZrO_2, and HfO_2 gate dielectrics was examined in [10], where HfO_2 demonstrated superior drain current (19.3μA) at higher gate voltages (0.6V) and approached the quantum capacitance limit. In another study, lanthanum oxide (La_2O_3) was proposed as a promising candidate due to its moderate permittivity and wide bandgap, providing improved electrostatic control for scaled devices [11]. Conversely, materials such as tantalum pentoxide (Ta_2O_5) have been shown to suffer from a narrow bandgap and low electron band offset with silicon, limiting their applicability [12]. Hafnium dioxide (HfO_2), by contrast, remains a prime candidate due to its high dielectric constant (~ 25), wide bandgap (~ 5.7Ev), and compatibility with silicon technology [13]. Additional developments have included the use of layered high-k structures to enhance dielectric breakdown strength [14], and the consideration of quantum capacitance as a critical parameter influencing total gate capacitance in nanoscale transistors [15]. However, prior studies have generally been limited in both the range of dielectric materials examined and the scope of performance parameters evaluated, leading to an incomplete understanding of their overall effects.

In this work, the performance of CNTFETs incorporating six different high-k dielectric materials; SiO_2, Al_2O_3, Y_2O_3, Ta_2O_5, HfO_2, and La_2O_3 was comprehensively evaluated. A comparative analysis was performed based on key electrical characteristics, including ON-state current, Quantum capacitance (QC), average carrier velocity, mobile charge per unit charge (mobile charge/q), Quantum-to-insulator capacitance ratio (QC/Cins), and transconductance-to-drain current ratio (gm/I_d). Simulations were carried out using the FETToy simulator available on the nanoHUB platform, a robust numerical modeling tool for ballistic MOSFET and CNTFET analysis.

1.1 DEVICE STRUCTURE

CNTFETs are proving to be one of the most promising nanoscale devices to implement advanced performance and densely integrated circuits with low energy consumption. In contrast to traditional MOSFETs, which use bulk silicon as the channel material, in CNTFETs, the channel is made by an individual carbon nanotube or even by an array of nanotubes. Their working principle is similar to that of MOSFETs in which electrons are injected via the source and collected via the drain, and the gate terminal controls the channel current, but the difference between the CNTFETs and the MOSFETs is the superior channel mobility exhibit by the CNTFETs. Their one-dimensional structure is unique and the carriers are confined to the cylindrical nanotube therefore strongly quantizing the electron and hole states. This allows the efficient transportation of charges in sub-bands in one-dimension at room temperature. In addition, the scattering phase-space is also smaller

which reduces the possibility of backscattering, which further adds to the exceptionally high conductivity of carbon nanotubes [10].

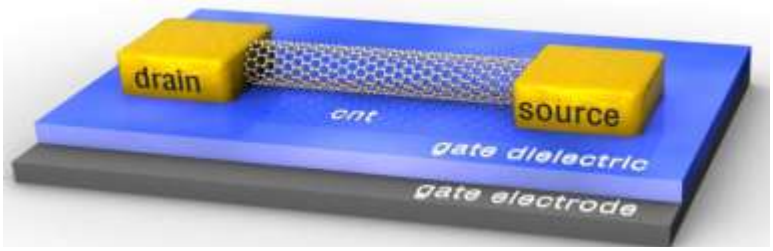

Figure 1: Carbon Nanotube Field Effect Transistor (CNTFET) [10]

The Carbon Nanotubes Transistors (CNTs) have all the bonds with the carbon atoms being completely filled and do not require any chemical passivation of the dangling bonds like silicon. As a result, the CNT-based electronics are not limited to silicon oxide as the insulating material. Rather, high dielectric constant and crystalline structure insulators can be used and thus three-dimensional device designs can be developed. The high thermal stability, covalent bonding, and resistance to electromigration of CNTs are due to the strong covalent bonding in CNTs giving rise to exceptionally high mechanical strength of CNTs. In contrast to traditional fabrication techniques, the nanotube diameter is a critical parameter, which is selected through chemical synthesis. As such, active devices (e.g., transistors) and metallic CNTs can both be produced in principle [16].

1.2 THEORETICAL BASIS

Dielectrics are commonly used as natural insulators in the storage of energy in electronic devices. High- k dielectrics are especially useful in capacitors, and the energy they store is quantified given by [17]:

$$U = \left(\frac{1}{2}\right) CV^2 \quad (1)$$

In equation (1), C represents the capacitance and V is the dielectric potential, which corresponds to the electric field since

$$E = \frac{-dv}{dl} \quad (2)$$

with dl as the differential length change in the material

It is indicated by Equation (1) that to optimise the energy storage within materials, either the capacitance (C) should be maximised or the applied potential/ electric field (V) should be maximised. For a parallel plate capacitor, capacitance could be maximized by minimizing the distance (d) or maximizing the plate area (A) as expressed by [17];

$$C = \frac{\varepsilon_o \varepsilon_r A}{d} \quad (3)$$

1.2.1 QUANTUM CAPACITANCE

Quantum capacitance is a material property that is similar to the Fermi level, and has been observed to lower the total capacitance in nanostructures very much against classical electrostatic expectations. This can be commonly termed as the dead layer effect of nanocapacitors and was first discovered as unexplained capacitance loss in dielectric thicknesses of atomic scale. Initial explanations of this effect attributed it erroneously to extrinsic influences, including fabrication defects, grain boundaries, or interface impurities. Recent research, however, has shown that even in highly optimized structures with pristine

interfaces the dead layer does not vanish but instead has a purely quantum mechanical basis [18].

In nanoelectronics, where dielectrics are of the order of a few atomic layers, classical electrostatics predicts very large capacitances. But experimental measurements of ultra-thin, defect-free oxide insulators are always below these theoretical expectations. To describe such discrepancy, the researchers usually refer to the so-called “dead layer” - which is in effect the modeling of the system as a large capacitance in series with the geometric capacitance. The total capacitance (C_G) observed is then found to behave as though the geometric capacitance (C_{geo}) has been in series with an additional component, the quantum capacitance (C_Q) which [19] expresses as:

$$\frac{1}{C_G} = \frac{1}{C_Q} + \frac{1}{C_{geo}} + \frac{1}{C_Q} \quad (4)$$

The geometric capacitance (C_{geo}) is much smaller than the quantum capacitance (C_Q) in most cases, and its impact can only be felt in nanoscale systems when the two can be compared in size. The quantum capacitance of the channel is especially important when the gate oxide capacitance (C_{OX}) is high (or when the Effective Oxide Thickness (EOT) is very thin) in further scaling. With the reduction in the size of the gates to nanoscale dimensions, the Density Of States (DOS) at the gate is limited, resulting in a direct relationship between the quantum voltage (V_Q) and gate charge (Q_G) as expressed in equation 5 given by [20]:

$$Q_G = \int_0^{V_Q} C_Q(V')dV' \quad (5)$$

CQ denotes the gate's quantum capacitance, which can be determined through Equation 5.

$$C_Q(V_Q) = q^2 \int_{-\infty}^{\infty} g(E)[-\frac{\partial f(E,E_{F,G})}{\partial E}]\text{dE} \quad (6)$$

The gate potential V_Q is equals to $-\left(\frac{E_{F,G}}{q}\right)$, where EF,G is the Fermi level of the gate with g(E) as the density of state, $f_{(E, EF,G)}$ as the Fermi-Dirac distribution, and q as the charge.
The physical thickness of the insulating layer has an inverse relationship with the capacitance of the insulating layer. In cases of a strong inversion, the capacitance of the inversion layer will usually prevail over the insulator capacitance. This results in a similarity in the total gate capacitance to the insulator capacitance [21]

2.0 METHODOLOGY

In this study, the FETToy simulator, a numerical modelling tool designed for ballistic MOSFET simulation, was employed to analyse the performance of CNTFETs. The simulated device adopts a MOSFET-like architecture with heavily doped source and drain regions. Device operation is governed by barrier height modulation through gate voltage control, where the drain current is determined by the gate-induced charge carriers within the channel. The study investigated the influence of high-k dielectric materials on CNTFET performance based on various parameters, including the current–voltage (I_d–V_g) characteristics, quantum capacitance, average carrier velocity, mobile charge, quantum-to-insulator capacitance ratio (Q_C/C_{ins}), and transconductance, all evaluated at 300K. For consistency, the nanotube diameter was set to 1 nm, the gate oxide thickness to 1.5nm, and a constant drain voltage of 1V was maintained for all simulations. Table 1 presents the six

different dielectric materials used as gate insulators in the CNTFET structure along with their respective relative dielectric constants.

Table 1: The six dielectrics

Name of gate dielectric material	Chemical formula	Dielectric constant
Silicon dioxide	SiO_2	3.9
Aluminium oxide	Al_2O_3	9
Yttrium(III) oxide	Y_2O_3	15
Tantalum (V) oxide	Ta_2O_5	22
hafnium oxide	HfO_2	25
Lanthanum oxide	La_2O_3	30

3.0 RESULTS AND DISCUSSION

This section presents the findings of the study on the influence of high-k dielectric materials on the performance of CNTFETs. The analysis focuses on key performance parameters, including drain current (I_d), quantum capacitance (Q_C), average carrier velocity, mobile charge per unit charge (mobile charge/q), quantum-to-insulator capacitance ratio (Q_C/C_{ins}), and transconductance-to-drain current ratio (gm/I_d).

3.1 DRAIN CURRENT VS GATE VOLTAGE

Figure 2 shows the i_d-v_g characteristics for carbon nanotube field effect transistor.

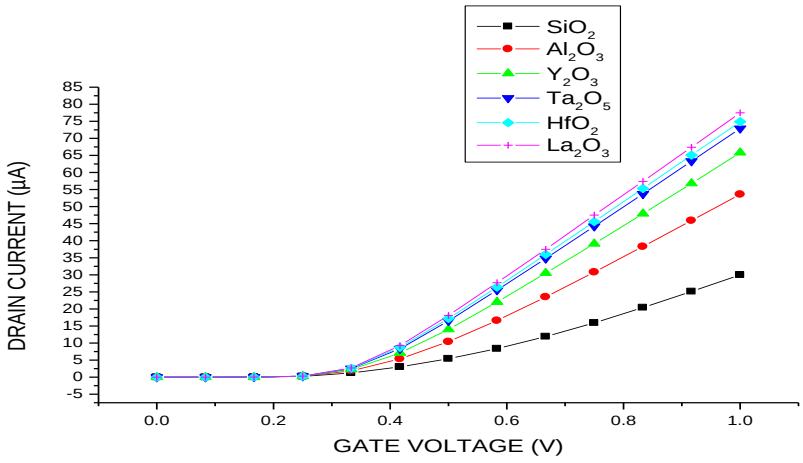

Figure 2: i_d–v_g characteristics of the CNTFET for six different gate dielectric materials.

This graph is a comparative performance of six high-k dielectric materials SiO_2, Al_2O_3, Y_2O_3, Ta_2O_5, HfO_2 and La_2O_3 on the effect on the i_d-v_g characteristic of the CNTFET. It was observed that the drain current (i_d) increased with both the dielectric constant of the gate material and the gate voltage (v_g). The materials that have been investigated include La_2O_3, HfO_2 and Ta_2O_5, which have a higher drain current value than the SiO_2 and Al_2O_3 which

performance is moderate. Particularly, La_2O_3 has the highest ON-current (77.5µA at V_g = 1V, V_{ds} = 1V), then Y_2O_3 (72.9µA), Al_2O_3 (74.9µA), Ta_2O_5 (65.8µA), and HfO_2 (53.6µA), and SiO_2 has the lowest ON-current (30µA) under the same bias conditions. High ON-current enables quicker switching, greater driving capacity, and enhanced device performance. High-k dielectrics enable efficient transfer of charge to the channel and reduce leakage currents by enhanced direct tunneling, and at the same time, a high gate capacitance is retained [20]. Higher ON-current represents superior performance [1]. Experimental findings prove the direct relationship between the gate dielectric permittivity (κ) and the of I-ON/I-OFF enhancement ratio. This enhancement is due to two reasons: (1) high on-state current and (2) low off state leakage, achieved using high-k dielectrics, attributed to more effective gate voltage channels modulation [7].

3.2 QUANTUM CAPACITANCE VS GATE VOLTAGE

Figure 3 shows how the quantum capacitance (C_q) varies with the gate voltage (V_g) at a constant drain voltage (V_{ds} = 1V) with insulator thickness 1.5nm of six different dielectric materials, i.e. SiO_2, Al_2O_3, Y_2O_3, Ta_2O_5, HfO_2, and La_2O_3

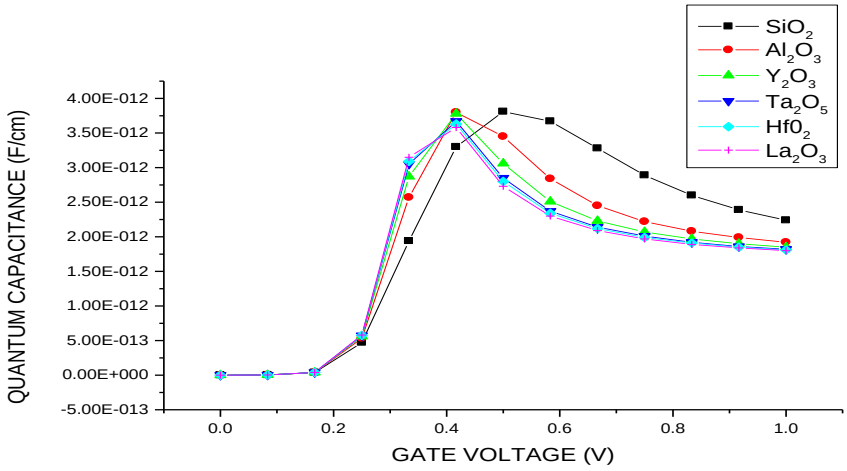

Figure 3: Quantum Capacitance Vs Gate Voltage for six different dielectric materials of CNTFET.

In Figure 3, the change in quantum capacitance (C_q) versus the gate voltage (V_g) of CNTFETs using the various high-k dielectric materials is shown. It was noted that C_q rises rapidly with increasing V_g between 0.2V and 0.5V, and gradually decreases above 0.5V with SiO_2, Al_2O_3, and Y_2O_3. The same trend was followed with Ta_2O_5, HfO_2 and La_2O_3 where C_q goes higher with V_g up to a certain point of about 0.41V and then decreases. SiO_2, which has a quantum capacitance of 2.24 x 10^{-12}F/cm, has the highest quantum capacitance, and La_2O_3 has the lowest quantum capacitance, which is 1.80 x 10^{-12}F/cm both at gate voltage of 1V. The difference in quantum capacitance may be explained by the difference in the density of states (DOS) and dielectric polarization of the respective materials. Materials with lower dielectric constant, such as SiO_2, are more likely to have greater quantum capacitance because of stronger electrostatic coupling between the channel and gate, and materials with

high dielectric constant such as La_2O_3 reduce effective gate control, resulting in a lower C_q. Such a behaviour shows the trade-off between dielectric constant and quantum capacitance to optimize the performance of CNTFET. The large quantum capacitance enhances the ability to control the gate and drive current through CNTFETs but values that are too large can increase dynamic power consumption. It is therefore crucial to choose a dielectric that provides a balance between C_q and C_{ox} to achieve an optimum performance in nanoscale CNTFETs.

3.3 AVERAGE VELOCITY VS GATE VOLTAGE

Figure 4 shows the graph of average carrier velocity against gate voltage (V_g) in CNTFET.

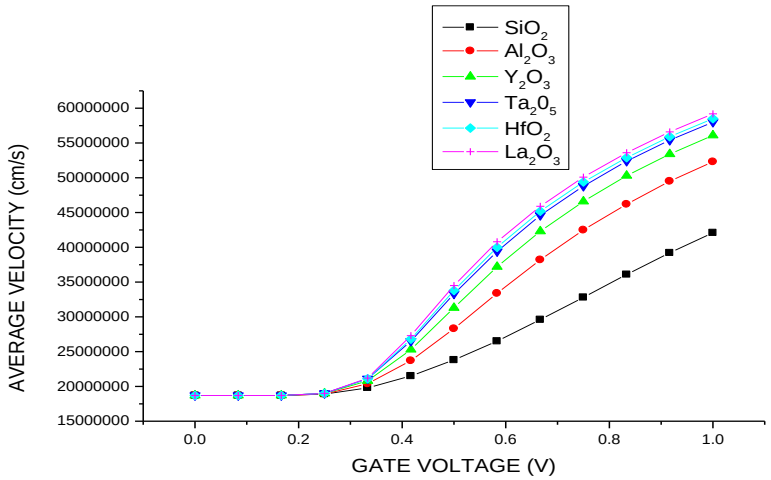

Figure 4: Average Velocity (cm/s) Vs Gate Voltage (v) of six different dielectric materials for CNTFET

Figure 4 illustrates the variation in average carrier velocity with the gate voltage (V_g) of CNTFETs where various dielectric materials have been used. It was noted that the average carrier velocity rises progressively with an increasing gate voltage, V_g. In all dielectric materials, the velocity was found to be almost constant up to 0.25V, after which it rises sharply above this voltage, indicating that carrier transport is improved by increased modulation of the gate. La_2O_3 exhibited the highest carrier velocity average of 5.92 $x10^6$cm/s, at a gate voltage of 1V, and SiO_2 showed the lowest carrier velocity average of 4.21 $x10^6$cm/s at the same bias condition. This highest carrier velocity of the La_2O_3 can be explained by the fact that La_2O_3 has higher dielectric constant, which leads to an increase in the electrostatic coupling and the decrease in the scattering effect phenomenon, which results in a better carrier transport efficiency in the CNT channel. On the other hand, the lower velocity of SiO_2 is due to its lower dielectric constant, which causes weak gate control and carrier acceleration. It has been demonstrated that increased carrier velocity increases current drive, transconductance and switching speed in CNTFETs resulting in optimal high frequency and low power operation.

3.4 MOBILE CHARGE PER CHARGE VS GATE VOLTAGE

Figure 5 shows how mobile charge per unit charge varies with the gate voltage (V_g) of CNTFETs using various dielectric materials. Mobile charge/q represents linear density of electrons in the channel which is a crucial parameter that defines the ability of the device to drive current.

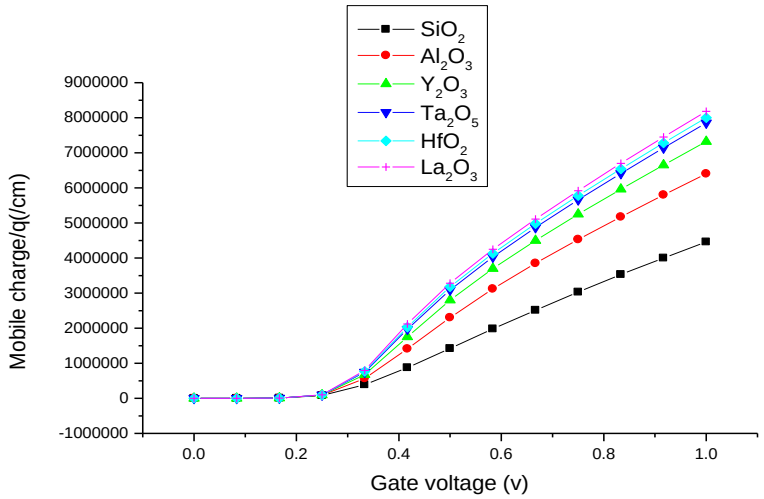

Figure 5: Mobile Charge/q Vs Gate voltage of six different dielectric materials for CNTFET

It can be pointed out from Figure 5 that there is a little or no significant change in mobile charge/q with respect to an increase in the gate voltage (V) when the voltage is below 0.3V. Mobile charge/q increases rapidly at an instant, together with the increase in the gate voltage(V) as the gate voltage exceeds 0.3V. It has also been noted that with an increase in the dielectric constant, the charge/q of the mobile charge also increases. A higher mobile charge/q/cm at a given gate voltage is an indicator of a strong gate control. The analysis of CNTFETs in terms of mobile charge/(q/cm) is not only a matter of convenience, but it is mandatory because of their inherently one-dimensional quantum. La_2O_3 has the highest (81.8×10^6) mobile charge/(q/cm) and SiO_2 has the lowest (4.46×10^6) mobile charge/(q/cm) at the same gate voltage of 1V.

3.5 QUANTUM CAPACITANCE PER INSULATOR CAPACITANCE VS GATE VOLTAGE

Figure 6 illustrates the change in quantum capacitance to insulator capacitance ratio (C_q/C_{ins}) and as a function of the gate voltage (V_g) of CNTFETs using various dielectric materials. The C_q/C_{ins} ratio is a non-dimensional parameter which indicates the relative contribution of the quantum capacitance to the total gate capacitance. As can be seen in the figure 6, the higher the dielectric constant, the lower the C_q/C_{ins} ratio at a given gate voltage, which is a sign of reduced dominance of quantum capacitance as the more polarizable the gate insulator.

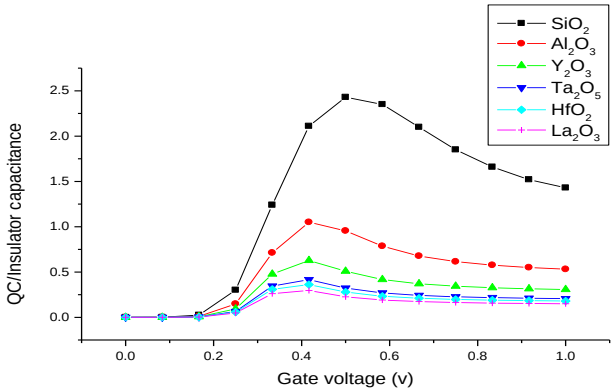

Figure 6: Quantum Capacitance/Insulator Capacitance Vs Gate voltage of six different dielectric materials for CNTFET

SiO_2 exhibits the highest ratio of quantum to insulator capacitance (C_q/C_{ins}) at 1.43, while $La_2\ O_3$ shows the lowest value of 0.15 at a gate voltage of 1V. It was also observed that, for each high-k dielectric material, the C_q/C_{ins} ratio increases with gate voltage, reaches a maximum, and subsequently decreases. This behavior indicates a transition in the dominant capacitance component from quantum capacitance to insulator capacitance as the gate voltage increases. Therefore, the selection of a suitable high-k dielectric material based on this parameter should be guided by the specific device application and its intended operating regime.

3.6 TRANSCONDUCTANCE PER DRAIN CURRENT VS GATE VOLTAGE

Figure 7 shows how transconductance per drain ratio (gm/I_d) changes with the gate voltage (V_g) at a given constant drain voltage (V_d) of 1V. It is noted that gm/I_d decreases continuously with the increase in the gate voltage. The maximum value of gm/I_d for all the six dielectric materials was attained at a gate voltage of less than 0.25V. The gm/I_d further declined as the gate voltage was increased. In the design of small-scale circuits, the gm/I_d ratio is an important figure of merit, because it establishes the trade-off between gain, speed and power efficiency. La_2O_3 was found to exhibit the highest value 29.7 $gm/I_d(/V)$, and SiO_2 exhibit the lowest 25.1V at the gate voltage 0.25V. A higher gm/Id value signifies enhanced current efficiency and superior transistor performance, which is desirable for low-power and high-gain applications.

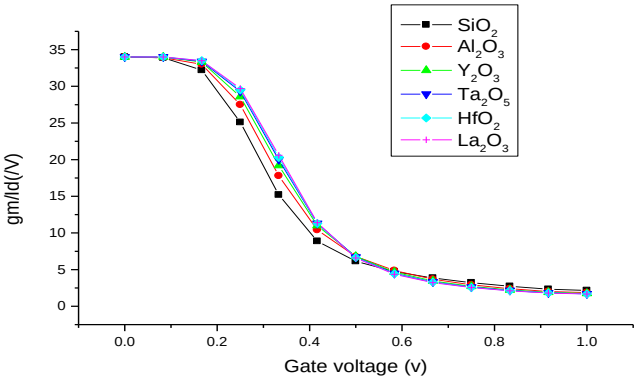

Figure 7: Gm/id vs Gate voltage of six different dielectric materials for CNTFET

4.0 CONCLUSION

The performance evaluation of CNTFETs with different high-k dielectric materials demonstrates a clear dependence of device behavior on the dielectric constant of the gate insulator. Across all examined parameters; drain current, quantum capacitance, carrier velocity, mobile charge, quantum-to-insulator capacitance ratio, and transconductance, the choice of dielectric material was found to significantly influence current drive capability and electrostatic control. The results demonstrated that dielectric materials with higher permittivity enhance device performance by improving gate coupling and charge transport efficiency. Among the investigated dielectric materials, $La_2\ O_3$ consistently exhibited the most favourable characteristics, including the highest ON-current, superior carrier velocity, and greater charge density, indicating strong gate modulation and efficient conduction in the CNT channel. In contrast, SiO_2 exhibited weaker performance across these parameters, emphasizing its limitations in advanced nanoscale transistor applications. Furthermore, the observed trade-off between dielectric constant and quantum capacitance underscores the importance of optimizing the dielectric selection to balance gate control, switching speed, and energy efficiency. The findings affirm that high-k dielectrics, particularly $La_2\ O_3$, hold substantial promise for next-generation CNTFET technologies, where enhanced current drive, low leakage, and energy-efficient operation are critical design priorities.

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